REMARKS

Claims 23-32, 38 and 42-51 are pending. The title, specification and claims are hereby amended.

The disclosure was objected to since the prior application data should be updated to reflect the issuance of U.S. Patent No. 6,818,993. The specification has been amended to attend to correction of this informality.

The Examiner objects to the title as not being descriptive of the claimed invention. The title has been amended to reflect the currently claimed subject matter.

Claim 23 was objected to due to a typographical error. This typographical error has been corrected by the present amendment.

Claims 23, 26, 30, 43 and 45-48 were rejected under 35 USC §102(b) as being anticipated by Hayashide. Favorable reconsideration of this rejection is requested in view of the amendments made herein.

Claim 23 reads on the structure of Fig. 23. In Fig. 23, the first insulating film 26 formed on the semiconductor substrate inclusive of the gate electrode and the source/drain regions, and the second insulating film 51 of a silicon nitride film formed on said first insulating film, constitute a first interlayer. Contact holes are formed through the first interlayer insulating layer, and plugs 29, for example, silicon, are formed filling the contact holes. The specification describes that silicon plug 29 is left in the contact hole 27 by etch-back or CMP (page 40, the

third paragraph). The upper surface of the plugs 29 is shown to be co-planar with, or to have a common surface with the upper surface of the second insulating film 51. A third insulating film 30 of silicon oxide is formed on the second insulating film 51 and the plugs 29, and a contact window 31 is formed therethrough, using the second insulating film 51 as an etch stopper.

Hayashide discloses an interlayer insulating film 17 comprising silicon oxide layers 5, 8, and 12 and a silicon nitride layer 9 (column 7, lines 18-22). Conductive plugs 14 are embedded in the contact holes penetrating through the first interlayer insulating film 17. The surface of the conductive plug 14 is at the level of the first interlayer insulating film, i.e., the surface of the oxide layer 12. The nitride layer 9 is not exposed on the surface of the first interlayer insulating film, and hence cannot be at the same level as the top surface of the conductive plug, and cannot serve as an etch stopper when an overlying insulating layer is to be etched. The Examiner cites the layer 10 as the third insulating film with conductive layer 15 but it is assumed the Examiner intended the oxide layer 18. The oxide layer 18 is formed to cover the conductive pattern 15.

Independent claim 43 reads on the structure of Fig. 32. Claim 43 requires said second insulating film having a surface coincident with the upper surface of said first insulating film. Hayashide does not disclose or suggest this structure.

Independent claim 45 reads on the structure shown in Fig. 31. Claim 45 requires the second insulating film as having a surface coincident with the upper surface of said first insulating film. Hayashide fails to teach or suggest this structure.

For at least the foregoing reasons, it is respectfully submitted that the presently claimed invention clearly distinguishes over Hayashide. Favorable reconsideration is earnestly solicited.

Claims 24, 25, 27-29, 31, 32, 44 and 49-51 were rejected under 35 U.S.C. §103 (a) as obvious over Hayashide and Fukuda et al.

Fukuda et al. can be overcome as prior art since a verified English language translation of the priority document had been filed in the parent application. The present application claims priority from an application filed July 18, 1996, which is prior to the PCT publication date of May 1, 1997 of Fukuda et al.

A verified English language translation of the priority application was filed in related application No. 10/050,169. A copy of the verified English language translation is available through PAIR in the file wrapper of the related application (now patent). Accordingly, Fukuda et al has been overcome as prior art.

Claims 38 and 42 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2 and 7 of U.S. Patent No. 6,344,692 in view of Fukuda et al. This rejection is rendered moot since Fukuda et al. has been overcome as prior art.

The Examiner's comments with respect to "product-by-process" limitations have been noted. With respect to claim 50, however, the phrase "made form the same conductive layer" would impart structural features in that a similar thickness and composition would be required.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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